不純物がつくる科学

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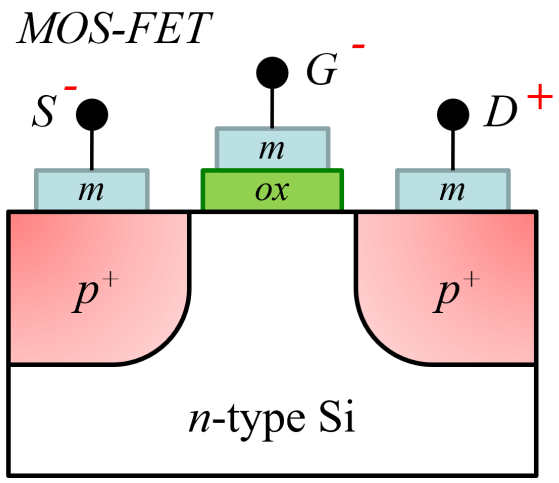
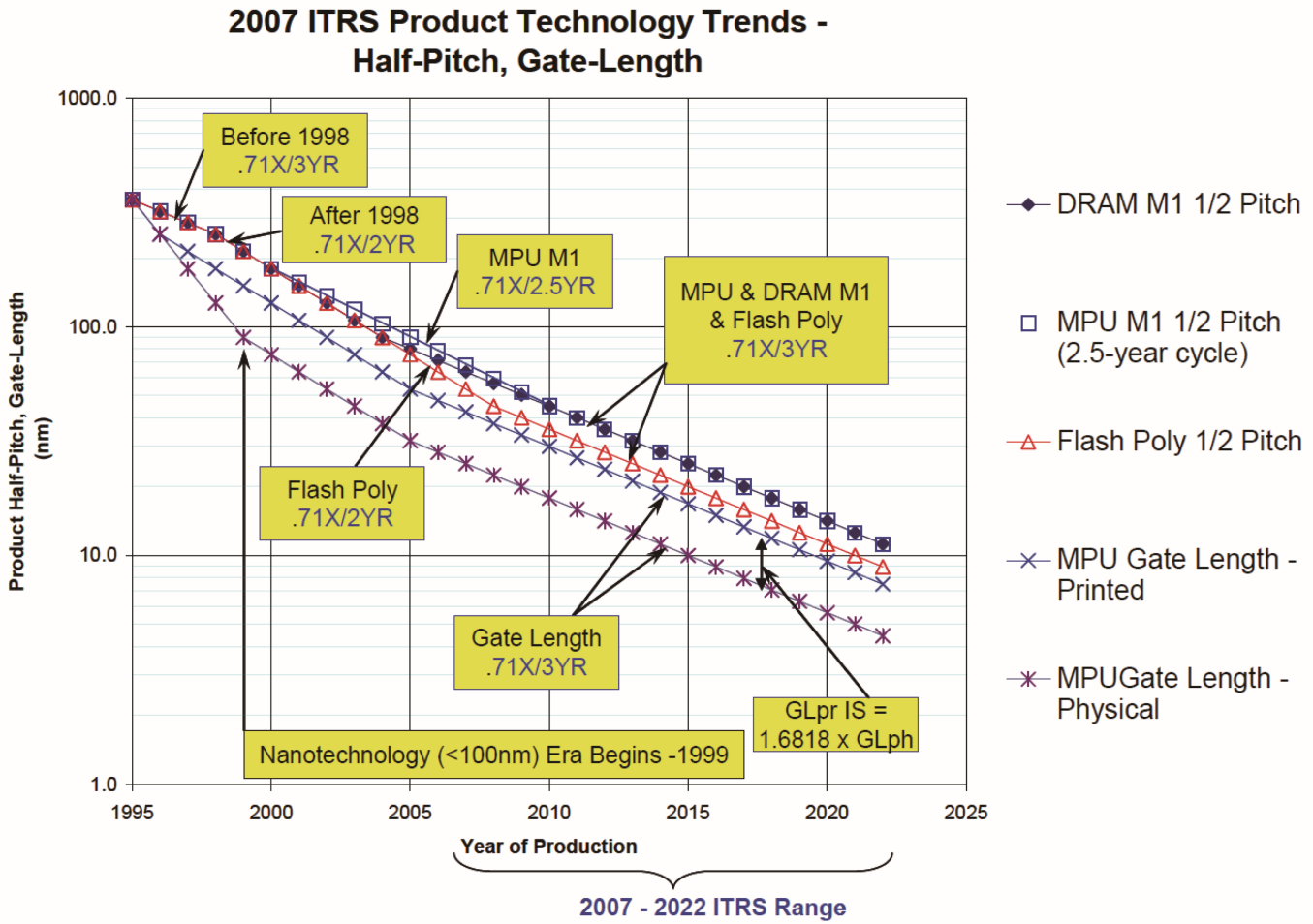
agenda

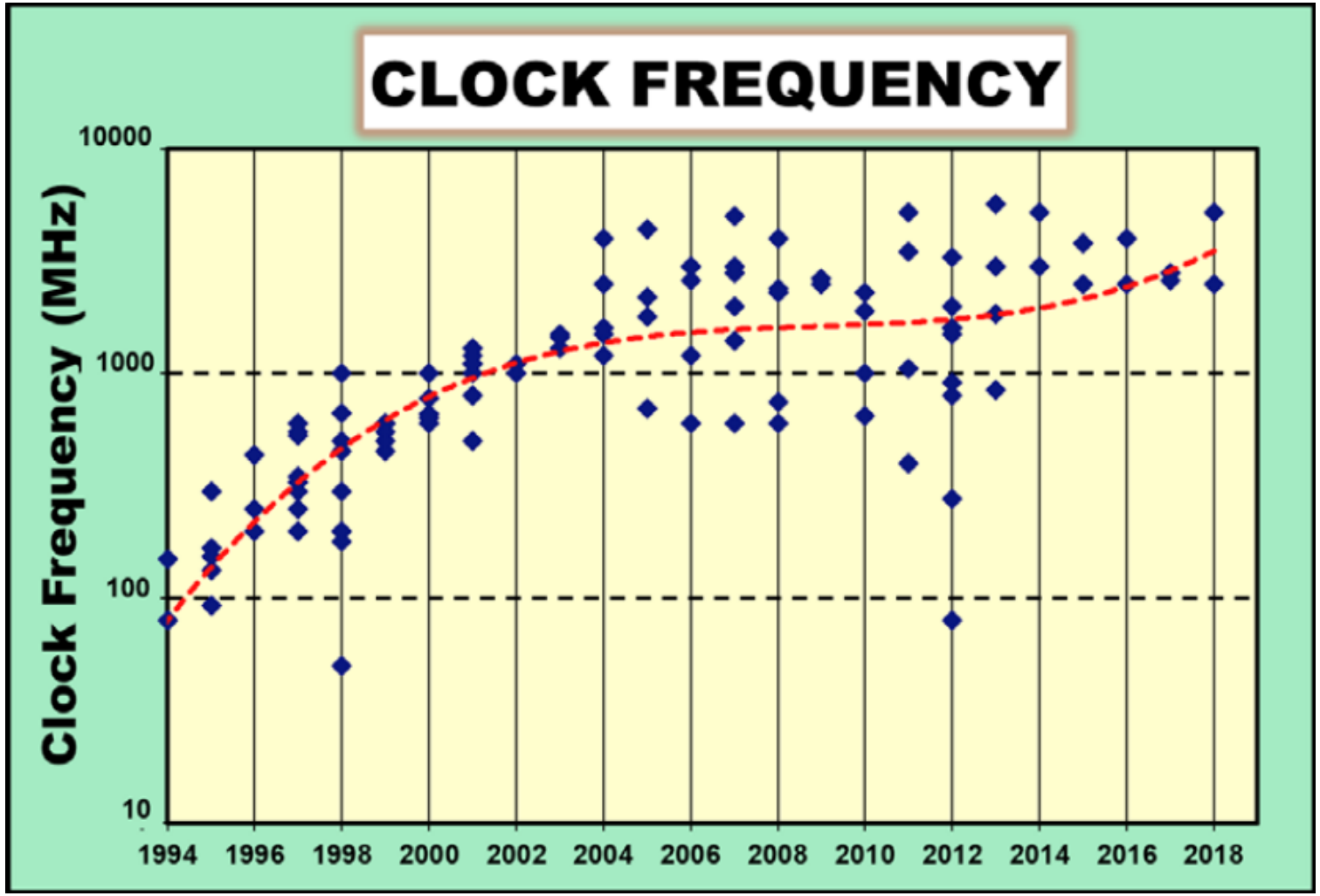
1. 最近の半導体事情
2. 半導体スピントロニクス
3. 量子コンピュータ
4. 不純物の科学
5. まとめ

MOSFET


MOS-FET
S -
G -
D +
m
ox
m
m
p+
p+
n-type Si


2007 ITRS Product Technology Trends -
Half-Pitch, Gate-Length
Product Half-Pitch, Gate-Length (nm)
1000.0
100.0
10.0
1.0
1995
2000
2005
2010
2015
2020
2025
Year of Production
2007 - 2022 ITRS Range
Before 1998
.71X/3YR
After 1998
.71X/2YR
MPU M1
.71X/2.5YR
MPU & DRAM M1
& Flash Poly
.71X/3YR
Flash Poly
.71X/2YR
Gate Length
.71X/3YR
GLpr IS =
1.6818 x GLph
Nanotechnology (<100nm) Era Begins -1999
DRAM M1 1/2 Pitch
MPU M1 1/2 Pitch
(2.5-year cycle)
Flash Poly 1/2 Pitch
MPU Gate Length -
Printed
MPUGate Length -
Physical

Clock frequency limited to less than 10GHz



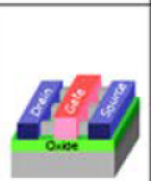
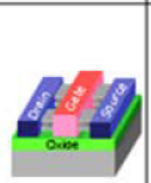
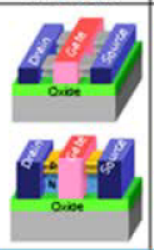
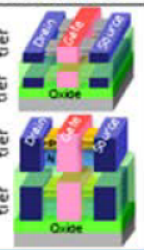
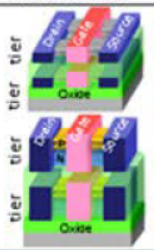
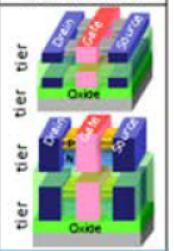
Scaling progressing

Logic/Foundry Process Roadmaps (for Volume Production)

	2016	2017	2018	2019	2020	2021	2022
Intel	14nm+	10nm (limited) 14nm++		10nm	10nm+	10nm++	7nm EUV
Samsung	10nm		8nm	7nm EUV 6nm EUV	18nm FDSOI 5nm	4nm	3nm GAA
TSMC	10nm	7nm 12nm		7nm+ EUV	5nm 6nm	5nm+	4nm 3nm
GlobalFoundries			22nm FDSOI 12nm finFET		12nm FDSOI	22nm+ FDSOI 12nm+ finFET	
SMIC				14nm finFET	12nm finFET	8-10nm finFET	
UMC		14nm finFET			22nm planar		

Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should only be seen as very general guidelines.

FinFET, transition to 3D geometry

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16 T2	G38M16 T4	G38M16 T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

Spin FET

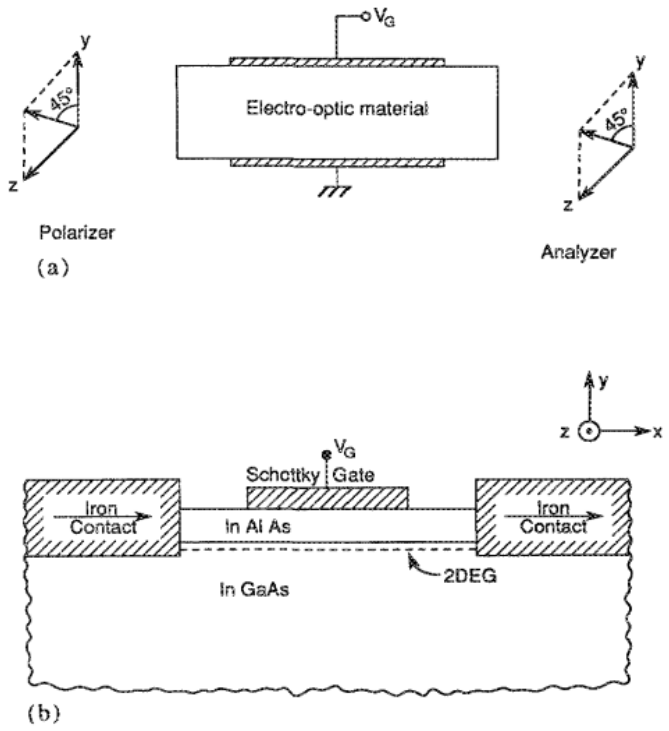


FIG. 1. (a) Electro-optic modulator; (b) proposed electron wave analog of the electro-optic modulator.

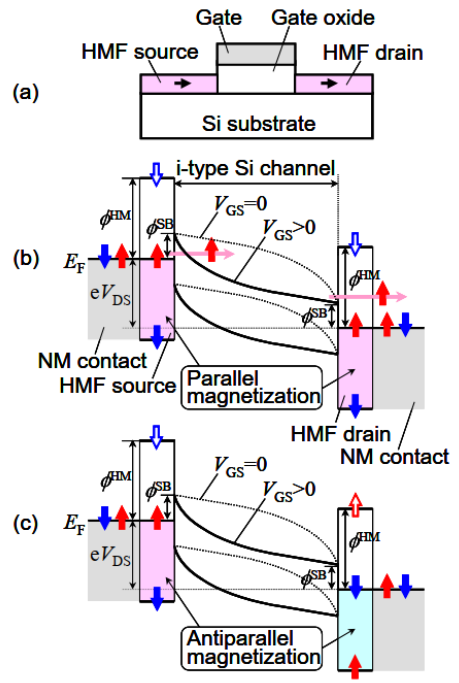


Fig. 1 Schematic (a) device structure and band diagrams of the spin MOSFET in (b) parallel and (c) antiparallel magnetization configurations.

Qubit register for Quantum Computing

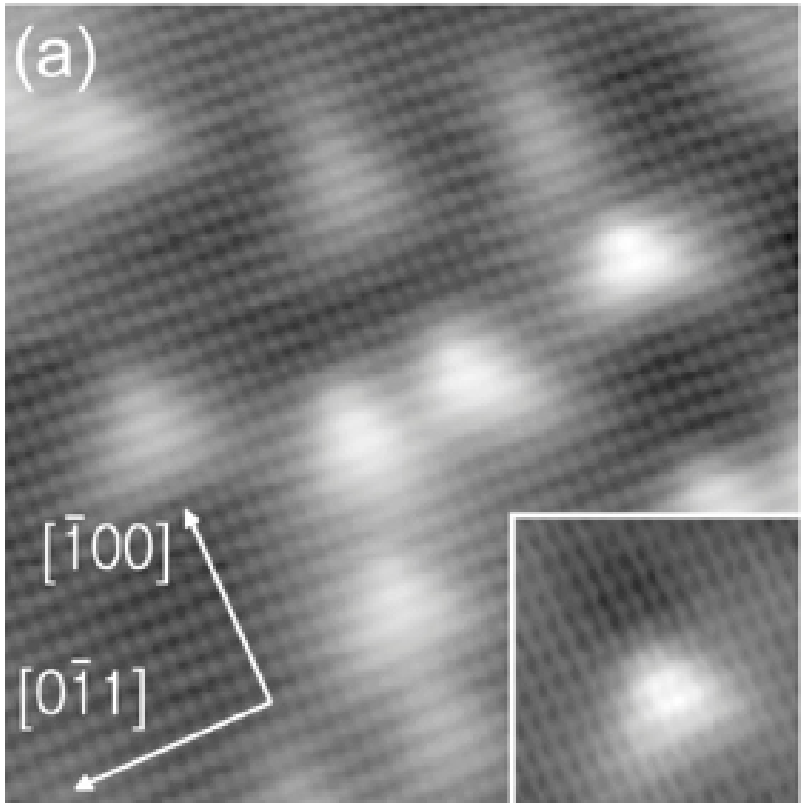
$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$$

- Superconductor
- Trapped ion
- Neutral atom
- **Quantum dot / well**
- **Silicon**
- **Diamond NVC**
- Non-linear / Linear optics
    - Many other medhods have been proposed.

Science of "Impurity"

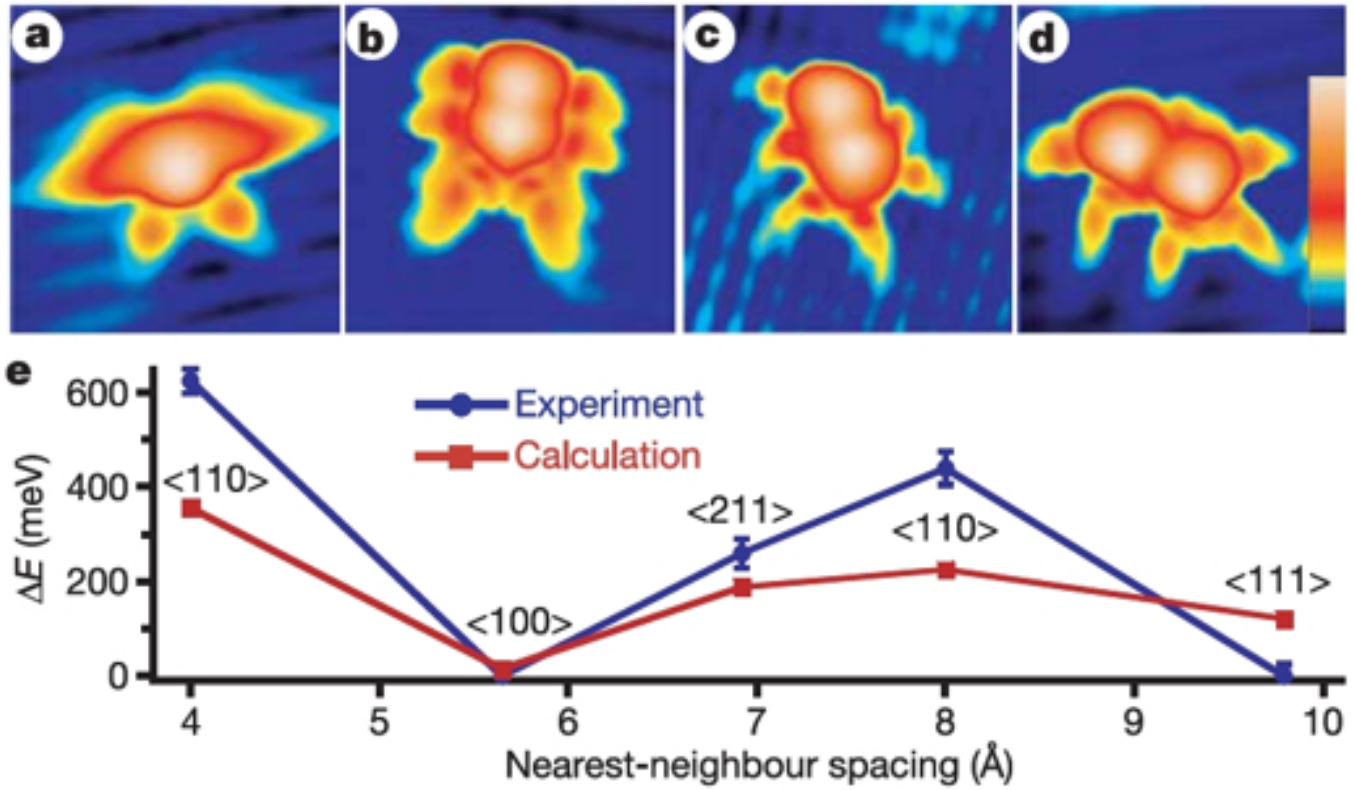
- いままで
  - 教科書的には不純物の状態は等方的に広がっているはず
  - 不純物の空間分布は無視できる、不純物まわりの不純物状態の広がりが大きい
  - 境界の効果は無視できる、バルク領域の方が大きい
- これから
  - サイズが小さくなれば、無視していたものも考慮に入れなければならない
  - 観測可能な領域にある＝境界の影響も考慮しなければならない

Impurity State "at Surface"



Zn(Be):GaAs(110)

Impurities "on Surface"



Mn pair on GaAs(110)

Kitchen, Nature 442, 436 (2006)

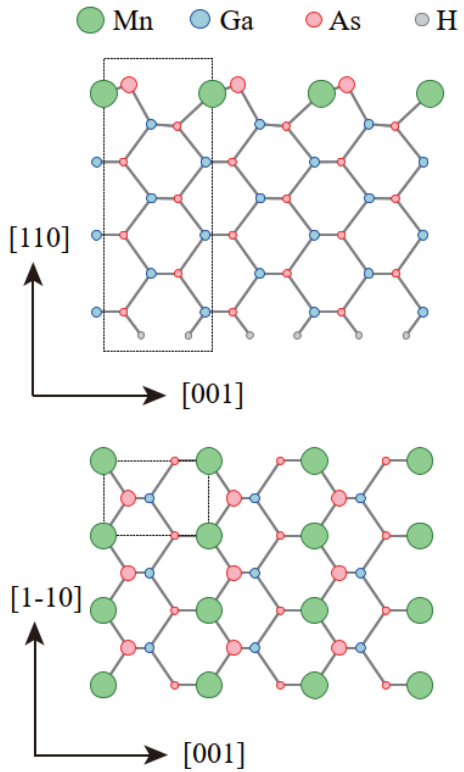
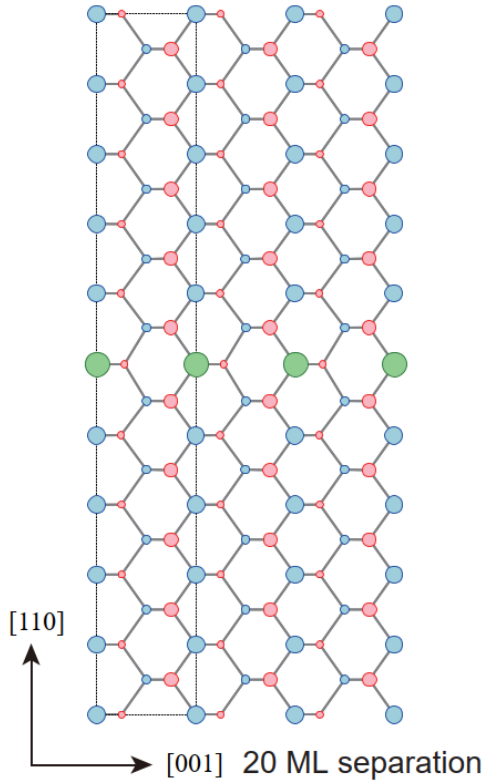
Impurity at "Surface" or "Interface"

- Spacial distribution of impurity state
- Interaction of impurity & surface/interface

Magnetism

- Direct exchange interaction (AFM favors)
- Indirect exchange interaction
  - Super-exchange mechanism (AFM favors)
  - Double exchange mechanism (FM favors)
  - Ruderman-Kittel-Kasuya-Yosida (RKKY) exchange mechanism (distance dependence)

Mn-(V) Molecular Layer on/in Semiconductor

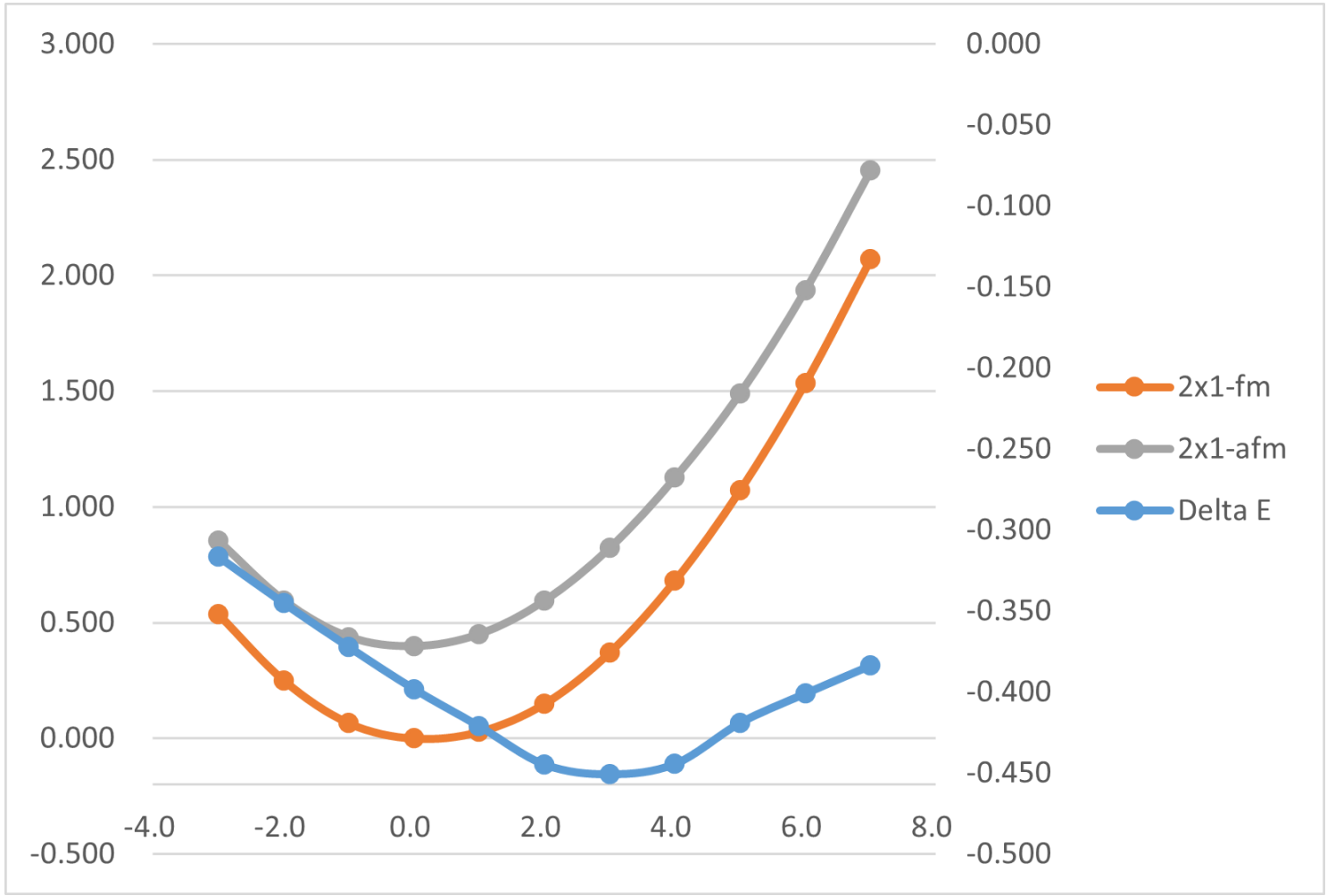
Surface	Bulk
	

Surface Spintronics

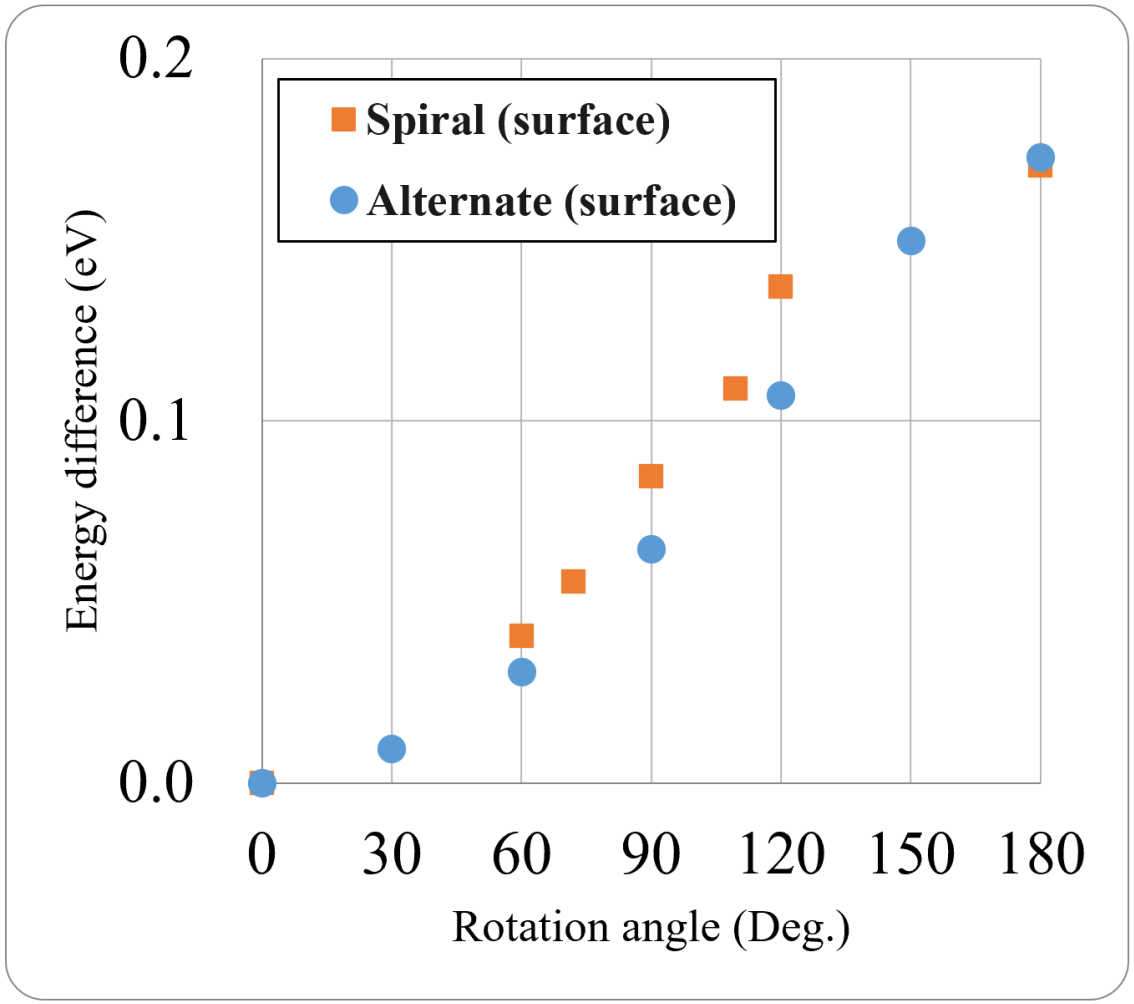
Mn-(V) molecular layer on surface

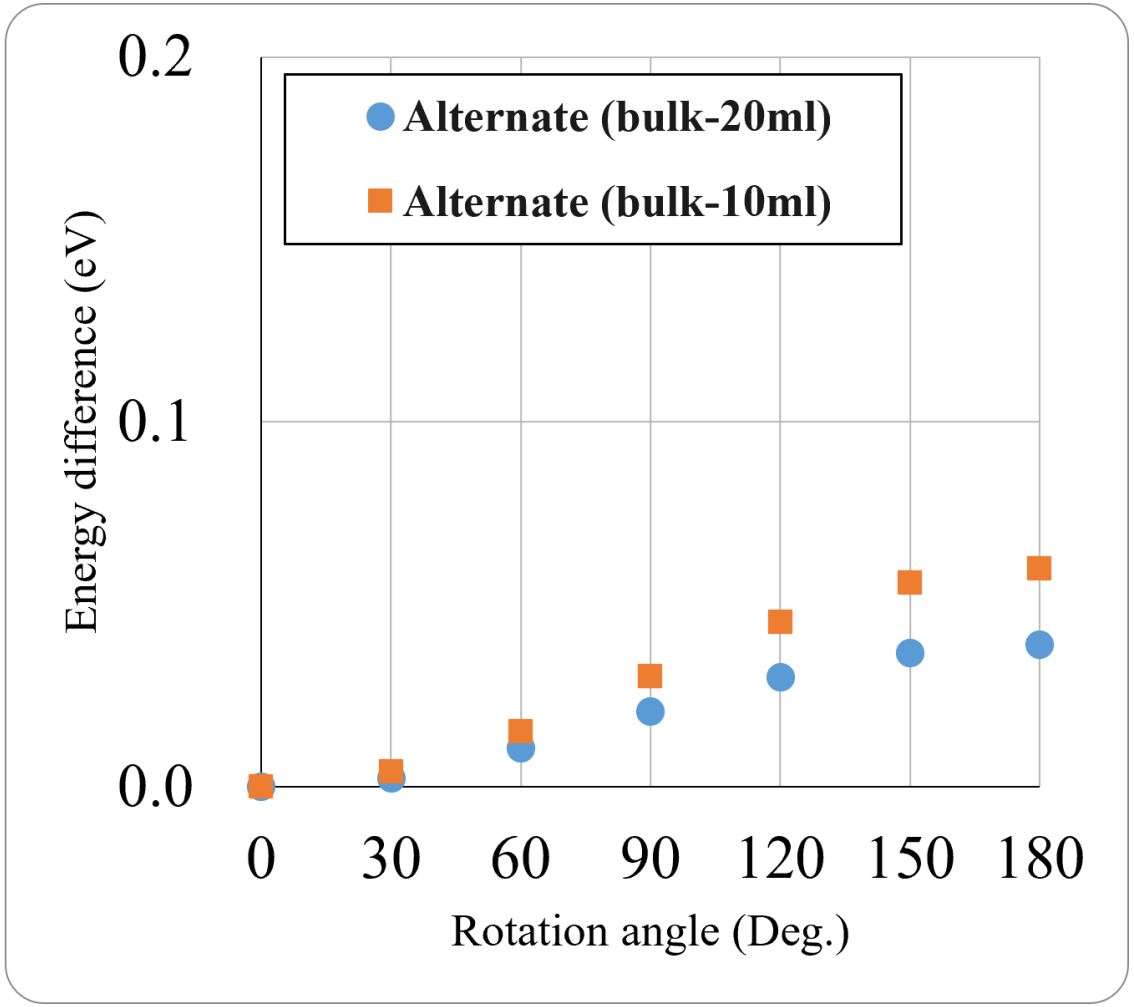
Host Material	Stable State	Mechanism
GaAs(110) GaP(110)	1D half-metal	Double exchange
GaN(110) GaSb(110)	2D half-metal	Double exchange
GaN$(1\bar{1}00)$	Metal	Direct/Double exchange
GaN$(11\bar{2}0)$	Semiconducting	Direct/Double exchange
BN(110)	Hounds-tooth AFM	Direct/Double exchange

Strain-reinforced ferromagnetism



Spin-orbit interaction (Relativistic effects)





まとめ

不純物は半導体の名わき役

実は知られていないことがたくさんある

未来の技術を作っていく

かもしれない